intel

iSBC® 286/10 PRODUCT FAMILY DATA BOOK

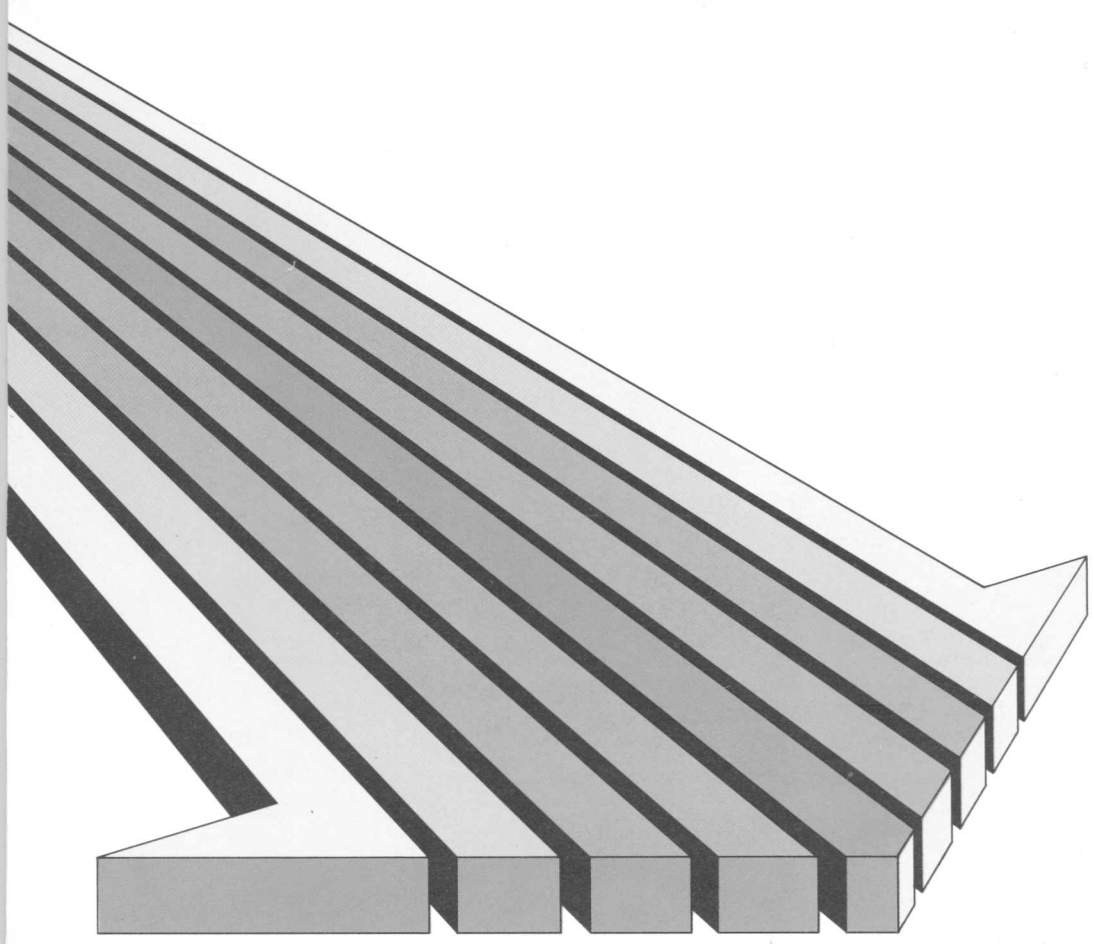
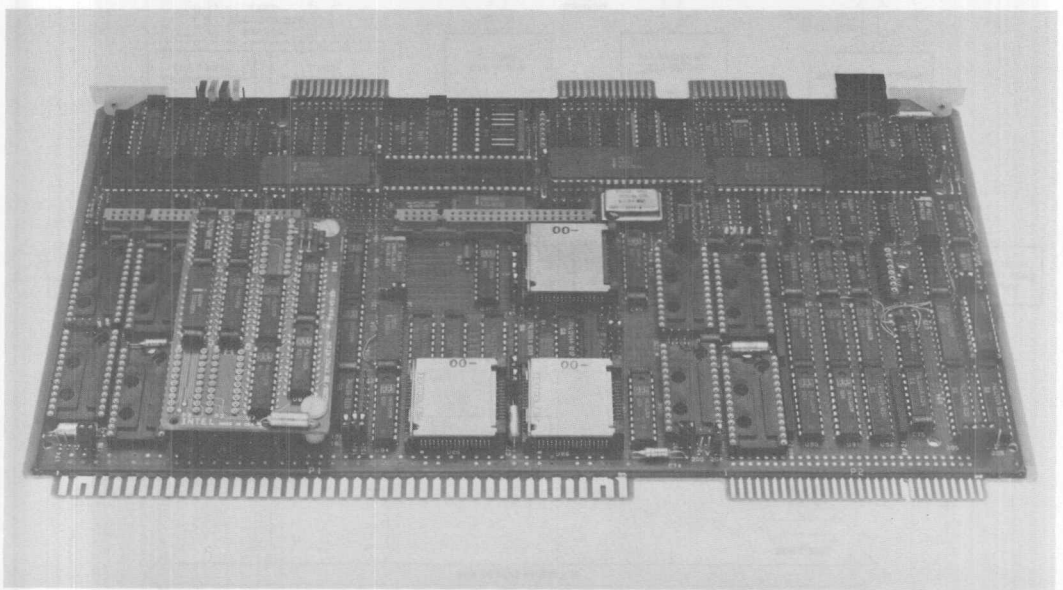


Table of Contents

iSBC® 286/10 SINGLE BOARD COMPUTER

- iAPX 286/10 (80286) Microprocessor with 6.0 MHz CPU clock
- Optional 80287 Numeric Data Processor
- iLBX™ (Local Bus Extension) interface for high-speed memory expansion
- Two iSBX™ bus interface connectors for I/O expansion
- Eight JEDEC 28-pin sites for optional RAM/iRAM/EPROM/E²PROM components
- Optional expansion to twelve JEDEC 28-pin sites with an iSBC® 341 28-pin site expansion board
- 16 levels of vectored interrupt control
- Centronics-compatible parallel I/O printer interface
- Two programmable multiprotocol synchronous/asynchronous serial interfaces; one RS232C, the other RS232C or RS422 compatible
- MULTIBUS® interface for multimaster configurations and system expansion

The iSBC® 286/10 Single Board Computer is a member of Intel's complete line of microcomputer modules and systems which take advantage of Intel's VLSI technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete microcomputer system on a 6.75 x 12.0 inch printed circuit card. The CPU, system clock, memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The iSBC 286/10 board is the first single board computer to incorporate the iAPX 286 CPU and the iLBX™ bus extension. This combination provides the highest performance 16-bit microcomputer system solution. The iLBX architectural expansion maintains this high performance for applications requiring vast amounts of system memory.



FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/10 board utilizes the powerful iAPX 286 CPU within the MULTIBUS system architecture, enhanced by the iLBX bus, to provide a high performance 16-bit solution. This board also includes on-board interrupt, memory and I/O features facilitating a complete single board computer system.

Central Processing Unit

The central processor for the iSBC 286/10 board is the 80286 CPU operating at a 6.0 MHz clock rate. The 80286 CPU is upwardly compatible with Intel's iAPX 88 and iAPX 86 CPUs. The 80286 CPU runs iAPX 88 and 86 code at substantially higher speeds due to a parallel chip architecture. In addition, the 80286 CPU provides on chip memory management and protection and virtual memory addressing of up to 1 gigabyte per task. Numeric processing power may be enhanced with the optional 80287 numerics processor. The clock rates for the 80286 and the 80287 are independent with the 80287 rate jumper selectable at either 4.0 or 8.0 MHz.

Instruction Set

The 80286 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the 80287 Numeric Data Processor extends the 80286 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The 80287 meets the proposed IEEE P754 standard for numeric data processing and maintains compatibility with 8087-based systems.

Architectural Features

The iAPX 86, 88, 186, and 286 CPU family all contain the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088 and 80186 CPUs.

The 80286 operates in two modes: iAPX 86 real address mode and protected virtual address mode. In iAPX 86

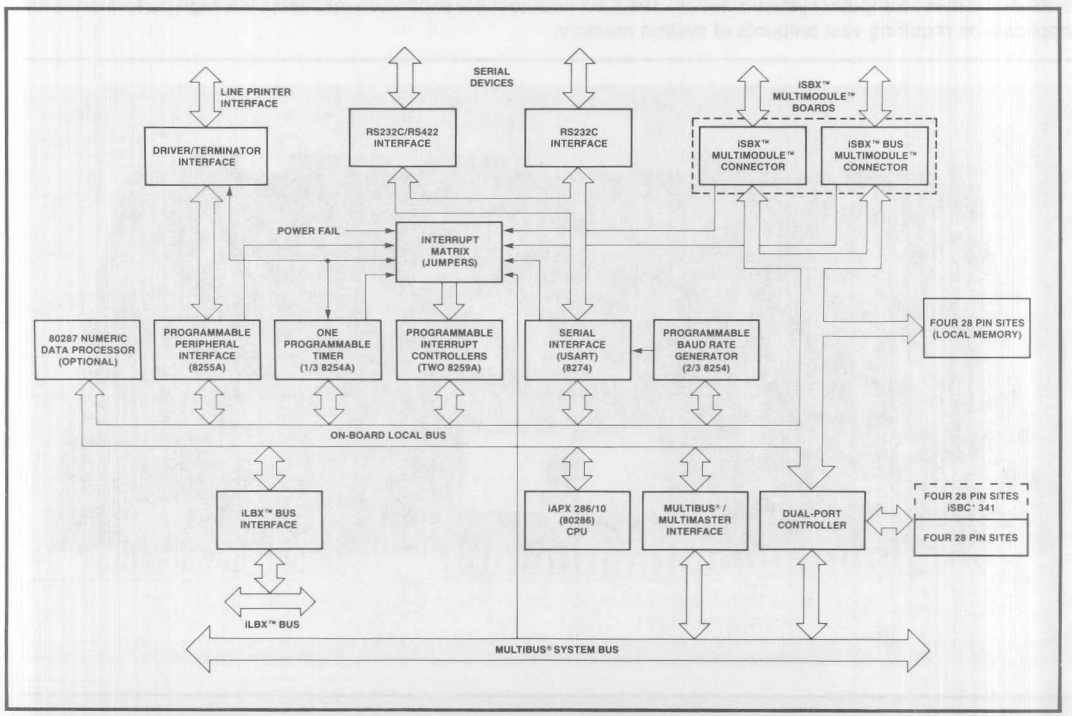


Figure 1. iSBC® 286/10 Block Diagram

real address mode, programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each tasks' programs and data. Both modes provide the same base instruction set, registers, and addressing modes.

VECTORED INTERRUPT CONTROL

Incoming interrupts are handled by two on-board 8259A programmable interrupt controllers and by the 80286's NMI line. Interrupts originating from up to 16 sources are prioritized and then sent to the CPU as a vector address. Further interrupt capability is available through bus vectored interrupts where slave 8259 interrupt controllers resident on separate SBC boards and are cascaded into the on-board interrupt control.

INTERRUPT SOURCES

Twenty-three potential interrupt sources are routed to the interrupt jumper matrix where the user can connect the desired interrupt sources to specific interrupt levels. Table 1 includes a list of devices and functions supported by interrupts.

MEMORY CAPABILITIES

There are eight 28-pin JEDEC sites on-board which may contain a combination of byte-wide devices including RAM, iRAM, EPROM, and E^2PROM. These sites are organized into two 4-site blocks, one of which may be dual-ported. The dual port block may be extended to eight sites (i.e. 12 sites total) by the addition of an iSBC 341 JEDEC site expansion module. The on-board EPROM capacity using twelve 27128 EPROMs is 192 Kbytes. The on-board RAM using ten 8K x 8 RAMs is 80 Kbytes.

SERIAL I/O

A two channel serial communications interface using Intel's 8274 Multi-Protocol Serial Controller (MPSC) is contained on the iSBC 286/10 board. Two independent software selectable baud rate generators provide the MPSC with all common communication frequencies. The protocol (i.e. asynchronous, IBM bisync, or SDLC/HDLC), data format, control character format, parity and baud rate are all under program control. Software interfacing to the MPSC can be via either a polled or interrupt driven routine. One channel may be configured for an RS232C or RS422 interface with the other channel RS232C only. The data, command and signal ground lines for each channel are brought out to two 26-pin connectors.

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS® interface	Requests from MULTIBUS® resident peripherals or other CPU boards	8*
8259A programmable interrupt controller	8 level vectored interrupt request cascaded to master 8259A	1
8274 serial controller	8 level vectored interrupt request cascaded to master 8259A	1
8255A line printer interface	Signals output buffer empty	1
8254 timers	Timer 0, 1 outputs; function determined by timer mode	2
iSBX™ connectors	Function determined by iSBX™ MULTIMODULE™ board	4 (2 per iSBX™ connector)
Bus fail safe timer	Indicates addressed MULTIBUS® resident device has not responded to command within 6 msec	1
Power fail interrupt	Indicates AC power is not within tolerance	1
External interrupt	General purpose interrupt from auxiliary connector, commonly used as front panel interrupt	1
On-board logic	Conditioned interrupt source from edge sense latch, inverter, or OR gate	3

* May be expanded to 56 with slave 8259A PICs on MULTIBUS® boards

PROGRAMMABLE TIMERS

The iSBC 286/10 board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller or to the 8274 MPSC to count external events or provide baud rate generation. The third interval timer in the 8254 is dedicated to providing a clock for the programmable baud rate generator in the iSBC 286/10 board's MPSC serial controller. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

LINE PRINTER INTERFACE

An 8255A Programmable Peripheral Interface (PPI) provides a line printer interface, several on-board functions, and four non-dedicated input bits. Drivers are provided for a complete Centronics compatible line printer interface. The on-board functions implemented with the PPI are power fail sense, override, NMI mask, non-volatile RAM enable, clear timeout interrupt, LED 0 and 1, clear edge sense flop, MULTIBUS interrupt, and serial channel A loopback. The PPI's I/O lines are divided into three eight bit ports: A, B and C. Four non-dedicated input bits allow the state of four user configured jumper connections to be input. The PPI must be programmed for mode 0 with ports A and C used as outputs and port B as input. A "dummy" write to port B is used to set the iSBC 286/10 board to protected mode. The parallel port bit assignment is shown in Table 3.

Table 3. Parallel Port Bit Assignment

Port A — Output	
Bit	**Function**
0	Line Printer Data Bit 0
1	Line Printer Data Bit 1
2	Line Printer Data Bit 2
3	Line Printer Data Bit 3
4	Line Printer Data Bit 4
5	Line Printer Data Bit 5
6	Line Printer Data Bit 6
7	Line Printer Data Bit 7
Port B — Input	
Bit	**Function**
0	General Purpose Input 0
1	General Purpose Input 1
2	General Purpose Input 2
3	General Purpose Input 3
4	Line Printer ACK/ (Active Low)
5	Power Fail Sense/ (Active Low)
6	Line Printer Error (Active Hi)
7	Line Printer Busy (Active Hi)
Port C — Output	
Bit	**Function**
0	Line Printer Data Strobe (Active Hi)
1	Override/ (Active Low)
2	NMI Mask (0 = NMI Enabled)
3	Non-Volatile RAM Enable; Clear Timeout Interrupt/
4	LED 0 (1 = On); Clear Edge Sense Flop/
5	MULTIBUS® Interrupt (1 = Active)
6	Serial CHA Loopback (0 = Online, 1 = Loopback)
7	LED 1 (1 = 0n); Clear Line Printer Ack Flop/

MULTIBUS® System Architecture

OVERVIEW

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the MULTIMODULE™ expansion bus as shown in Figure 2. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The local bus extension alllows large amounts of high performance memory to be accessed from a CPU board over a private bus. The MULTIMODULE extension bus is a means of adding inexpensive I/O functions to a base CPU board. Each of these three bus structures are implemented on the iSBC 286/10 board providing a total system architecture solution.

SYSTEM BUS – IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations with multiple processors and intelligent slave, I/O and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

SYSTEM BUS – EXPANSION CAPABILITIES

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

SYSTEM BUS – MULTIMASTER CAPABILITIES

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 286/10 board provides full system bus arbitration control logic. This control logic allows up to three iSBC

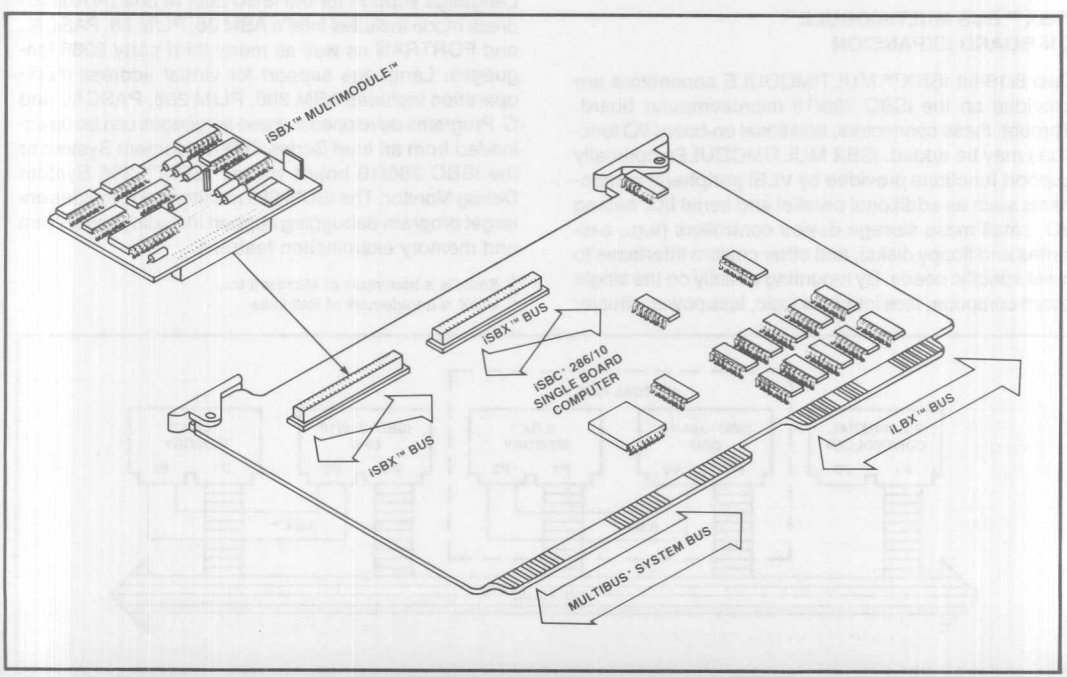


Figure 2. MULTIBUS® System Architecture

286/10 boards or other bus masters, including iSBC 80 family MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to multiprocessing configuration made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

iLBX™ BUS – LOCAL BUS EXTENSION

The iSBC 286/10 board also provides the local bus extension (iLBX) of the MULTIBUS architecture. This standard extension allows on-board memory performance with physically off-board memory. The combination of a CPU board and iLBX memory boards is architecturally equivalent to a single board computer and thus can be called a "virtual SBC". The iLBX is implemented over the P2 connector and requires cabling across the virtual SBCs of a system (see Figure 3). Other Intel products which support the iLBX bus include:

iSBC 028CX 128KB iLBX RAM board
iSBC 056CX 256KB iLBX RAM board
iSBC 012CX 512KB iLBX RAM board
iSBC 428 JEDEC 28-PIN SITE board
iSBC 580 MULTICHANNEL™ interface board

iSBX™ BUS MULTIMODULE™ ON-BOARD EXPANSION

Two 8/16-bit iSBX™ MULTIMODULE connectors are provided on the iSBC 286/10 microcomputer board. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULEs optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 286/10 board provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 286/10 microcomputer board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification and iSBX connectors are available from Intel.

Software Support

Real-time support for the iSBC 286/10 board is provided by the iRMX™ 286R operating system. iRMX 286R is an adaptation of iRMX 86 nucleus to operate on the iSBC 286/10 board in real address mode, enhances the ICU for configuration support of the board, adds a driver for the on-board 8274 and supports the 80287. The iRMX 286R Operating System is completely compatible with iRMX 86.

Interactive multi-user support will be provided by the XENIX[1] operating system. XENIX is a compatible derivative of UNIX[2], System III.

Language support for the iSBC 286/10 boards real address mode includes Intel's ASM 86, PL/M 86, PASCAL and FORTRAN as well as many third party 8086 languages. Language support for virtual address mode operation includes ASM 286, PL/M 286, PASCAL and C. Programs developed in these languages can be downloaded from an Intel Series III Development System to the iSBC 286/10 board via the iSDM™ 286 System Debug Monitor. The iSDM 286 monitor also provides on-target program debugging support including breakpoint and memory examination features.

1 Xenix is a trademark of Microsoft Inc.
2 UNIX is a trademark of Bell Labs.

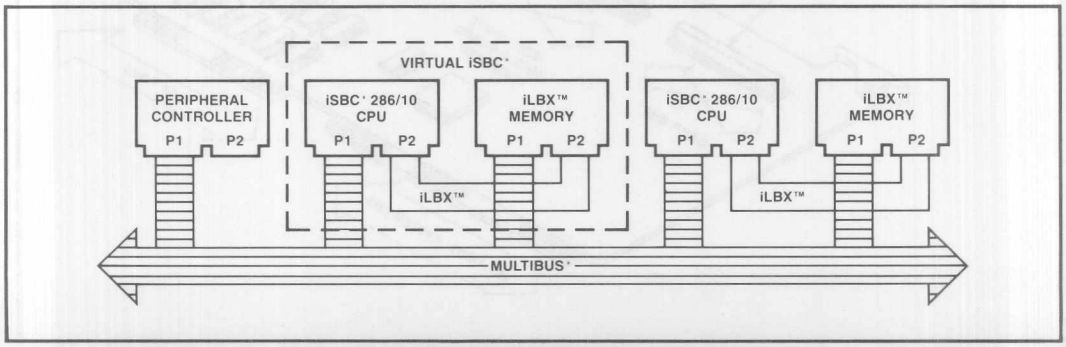


Figure 3. MULTIBUS®/iLBX™ Configuration

SPECIFICATIONS

Word Size

Instruction — 8, 16, 24, 32 or 40 bits

Data — 8 or 16 bits

System Clock

CPU — 6.0 MHz

Numeric Processor — 4.0 or 8.0 MHz (Jumper Selectable)

Cycle Time

Basic Instruction — 6.0 MHz - 500 ns; 333 ns (assumes instruction in queue)

NOTE: Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles).

Memory Capacity (Maximum)

EPROM — 2716, 8 Kbytes; 2732, 16 Kbytes; 2764, 64 Kbytes; 27128, 128 Kbytes; 27256, 256 Kbytes

E²PROM — 2817A, 16 Kbytes

iRAM — 2186, 16 Kbytes

Static RAM — 8K x 8 devices, 48 Kbytes

NOTES: Two local sites must contain boot-up EPROM or E²PROM. 2716s and 2732s may reside in dual-port sites only. iRAMs may reside in local sites only.

WITH iSBC® 341 MULTIMODULE™

EPROM — 2716, 16 Kbytes; 2732, 32 Kbytes; 2764, 96 Kbytes; 27128, 192 Kbytes; 27256, 256 Kbytes

E²PROM — 2817A, 24 Kbytes

iRAM — 2186, 16 Kbytes

Static RAM — 8K x 8 devices, 80 Kbytes

NOTES: Dual-port sites can address 128 Kbytes of memory maximum. Two local sites must contain boot-up EPROM or E²PROM. 2716s and 2732s may reside in dual-port sites only. iRAMs may reside in local sites only.

I/O Capability

Parallel — Line printer interface, on-board fuctions, and four non-dedicated input bits

Serial — Two programmable channels using one 8274

Timers — Three programmable timers using one 8254

Expansion — Two 8/16-bit iSBX MULTIMODULE connectors

Interrupt Capacity

Potential Interrupt Sources — 23, jumper selectable

Interrupt Levels — 16 vectored requests using two 8259As and the 80286's NMI line.

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity.

BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)				
	Synchronous	Asynchronous			
Reference: 1.23 MHz	÷1	÷1	÷6	÷32	÷64
615.	615,000	615,000	38,400	19,200	9,600
307.	307,000	307,000	19,200	9,600	4,800
154.	154,000	154,000	9,600	4,800	2,400
76.8	76,800	76,800	4,800	2,400	1,200
38.4	38,400	38,400	2,400	1,200	600
19.2	19,200	19,200	1,200	600	300
9.6	9,600	9,600	600	300	150
4.8	4,800	4,800	300	150	75
2.4	2,400	2,400	150	75	—
1.2	1,200	1,200	75	—	—
0.6	600	600	—	—	—

TIMERS

Input Frequencies — 1.23 MHz ±0.1% or 3.00 MHz ±0.1% (Jumper Selectable)

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-time interrupt	667 ns	53.3 ms	1.33 μs	58.2 min
Programmable one-shot	667 ns	53.3 ms	1.33 μs	58.2 min
Rate generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Square-wave rate generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Software triggered strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Hardware triggered strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Event counter	—	8.0 MHz	—	—

INTERFACES

MULTIBUS®— All signals TTL compatible

iSBX™ Bus — All signals TTL compatible

iLBX™ Bus — All signals TTL compatible

Serial I/O — Channel A: RS232C/RS422 compatible, configurable as a data set or data terminal; Channel B: RS232C compatible, configured as data set

Timer — All signals TTL compatible

Interrupt Requests — All TTL compatible

CONNECTORS

Interface	Double-Sided Pins (qty.)	Centers (in.)	Mating Connectors
MULTIBUS® System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
iSBX™ Bus — 8-Bit Data	36	0.1	iSBX™ 960-5
16-Bit Data	44	0.1	iSBX™ 961-5
iLBX™ Bus	60	0.1	Kelam RF30-2803-5 or T&B Ansley A3020 (609-6026 modified)
Parallel I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

MULTIBUS® DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	16
Address	Tri-State	16
Commands	Tri-State	32
Bus Control	Open Collector	20

iLBX™ DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	9
Address	Tri-State	20
Commands	Tri-State	8
Bus Control	TTL	8

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.70 in. (1.78 cm)

NOTE: Depth includes a small piggyback on lower left of board.

Weight — 19 oz. (539 gm)

Electrical Characteristics

DC Power Requirements — +5V, 7.0A; +12V, 50 mA; −12V, 50 mA

NOTE: Does not include power for optional EPROM, E²PROM, or RAM.

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Relative Humidity — to 90% (without condensation)

Reference Manual

145439-001 — iSBC 286/10 Single Board Computer Design Guide (NOT SUPPLIED)

ORDERING INFORMATION

Part Number	Description
SBC 286/10	Single Board Computer

iSBC® 028CX, 056CX, AND 012CX iLBX™ RAM BOARDS

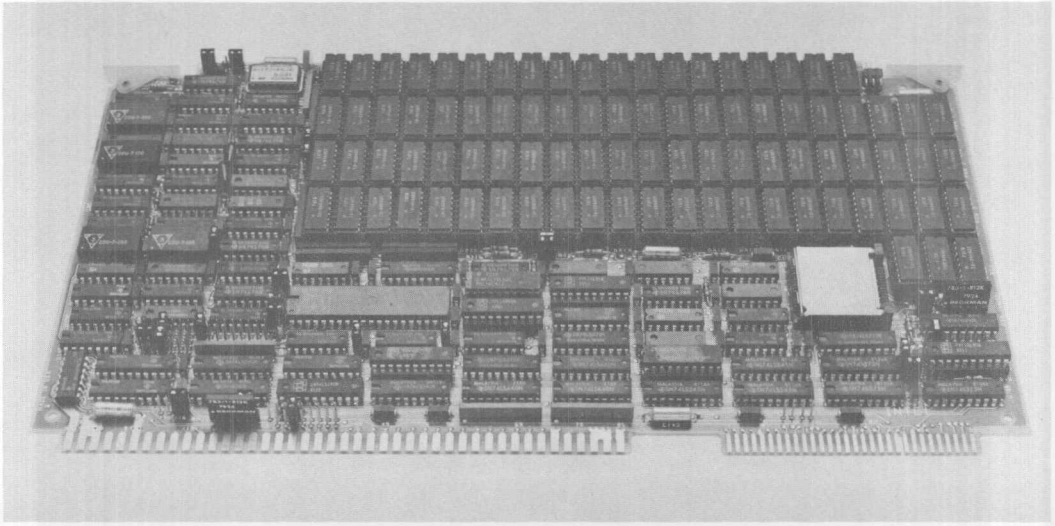
- **Dual port capability via MULTIBUS® and iLBX™ Bus Interfaces**
- **Single bit error correction and double bit error detection via Intel 8206 ECC device**
- **128K byte, 256K byte and 512K byte versions available**
- **Control status register supports multiple ECC operating modes**
- **Error status register provides error logging by host CPU board**
- **16 megabyte addressing capability with base address selectable on 16K byte boundaries**
- **Supports 8- or 16-bit data transfer and 24-bit addressing**
- **Auxiliary power bus and memory protect logic for battery back-up RAM requirements**

The iSBC® 028CX, iSBC 056CX, and iSBC 012CX RAM memory boards are members of Intel's complete line of iSBC memory and I/O expansion boards. Each board interfaces directly to any iSBC 80, iSBC 88, iSBC 86, iSBC 186 and iSBC 286 Single Board Computers. The dual port feature of the CX series of RAM-boards allows access to the memory of both the MULTIBUS® and the iLBX™ interfaces.

In addition to the dual port features the "CX" series of RAM-boards provide Error Correction Circuitry (ECC) which can detect and correct single bit errors and detect, but not correct, double and most multiple bit errors.

The iSBC 028CX, iSBC 056CX and iSBC 012CX boards contain 128K, 256K or 512K bytes of read/write memory using 64K dynamic RAM components.

Due to the iLBX dual port capability and on-board ECC features of the board they are ideally suited in applications where memory performance and integrity of the stored data is critical, such as financial transactions, process control and medical equipment applications.



FUNCTIONAL DESCRIPTION

General

The iSBC 028CX, 056CX and 012CX RAM boards are physically and electrically compatible with the MULTIBUS interface standard, IEEE P796, as outlined in the Intel MULTIBUS specification. In addition the CX series of RAM-boards are physically and electrically compatible with the iLBX bus interface as outlined in the Intel iLBX Specification.

Dual Port Capabilities

The "CX" series of RAM-boards can be accessed by either the MULTIBUS interface or the iLBX interface. Intel's new Local Bus Extension interface (iLBX bus) is an unarbitrated bus architecture which allows direct transfer of data transfer between the CPU and the memory boards without accessing the MULTIBUS. Due to the unarbitrated nature of the iLBX interface significant improvements in memory access times result, typically 350% to 400%, over MULTIBUS memory access times.

System Memory Size

Maximum system memory size with this series of boards is 16 megabytes. Memory partitioning is independant for the MULTIBUS interface and the iLBX interface.

For MULTIBUS operations, on-board jumpers assign the board to one of four 4-megabyte pages. Each page is partitioned into 256 blocks of 16K bytes each. The smallest partition on any board in this series is 16K bytes. Jumpers assign the base address (lowest 16K block) within the selected 4-megabyte page.

The iLBX bus memory partitioning differs from the MULTIBUS partitioning in that the iLBX bus address space consists of 256 contiguous blocks of 64K bytes totaling 16 megabytes. As with the MULTIBUS partitioning the base addresses are set with on-board jumpers.

Error Checking and Correcting (ECC)

Error checking and correction is accomplished with the Intel 8206 Error Checking and Correcting device. This ECC component in conjunction with the ECC check bit RAM array provides error detection and correction of single bit errors and detection only of double bit and most multiple bit errors. The ECC circuitry can be programmed via the Control Status Register (CSR) to various modes while error logging is supported by the Error Status Register (ESR). Both CSR and ESR communicate with the master CPU board through a single I/O port.

ECC I/O ADDRESS SELECTION

The processor board communicates with the ECC circuitry via a single I/O port. This port is used for the Control Status Register (CSR) and the Error Status Register (ESR). The CSR is programmed by the user to determine the mode of operation while the ESR provides information about memory errors. The iSBC 028CX, iSBC

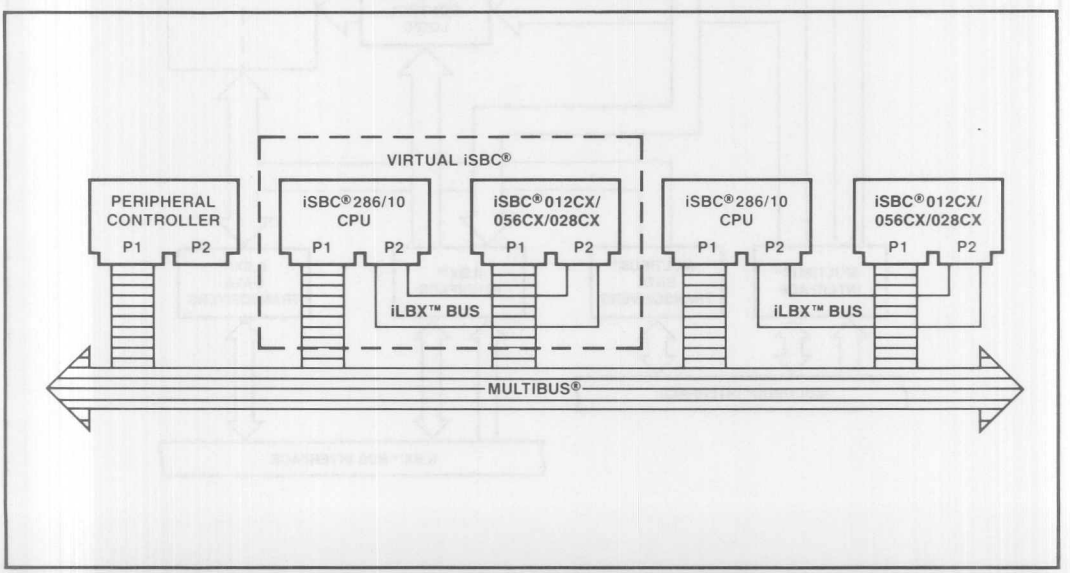


Figure 1. Typical iLBX™ System Configuration

256CX and iSBC 012CX RAM boards are shipped with a Programmed Array Logic (PAL) device which allows selecting one of 9 possible addresses for the I/O port. The actual selection is done by jumper configuration. Additional unprogrammed locations are left in the PAL to allow application specific I/O addresses to be defined.

CONTROL STATUS REGISTER

There are six ECC modes of operation in the "C" Series family of RAM boards. Each mode is obtained by software programming of the CSR from the master iSBC board. The six modes are:

a. Interrupt on any error mode
b. Interrupt on non-correctable error only mode
c. Correcting mode
d. Non-correcting mode
e. Diagnostic mode
f. Examine syndrome word mode

Modes (a) and (b) can be used in conjunction with (c) and (d). The six modes are described below.

Interrupt on Any Error Mode — In this mode the RAM board will interrupt the iSBC processor board when any error (single bit or multiple bit) is detected by the ECC circuitry.

Interrupt on Non-Correctable Error Mode — In this mode the RAM board will interrupt the iSBC processor board only when a non-correctable (multiple bit) error is detected by the ECC circuitry. A multiple bit error is not correctable by the ECC circuitry.

Correcting Mode — In this mode the RAM board corrects any correctable error (single bit error). Errors which are not correctable are not modified. Interrupts are generated depending on the interrupt mode selected.

Non-Correcting Mode — In this mode the RAM board does not correct any error. The ECC circuitry continues to check for errors, but no corrective action is taken. Interrupts continue as described previously.

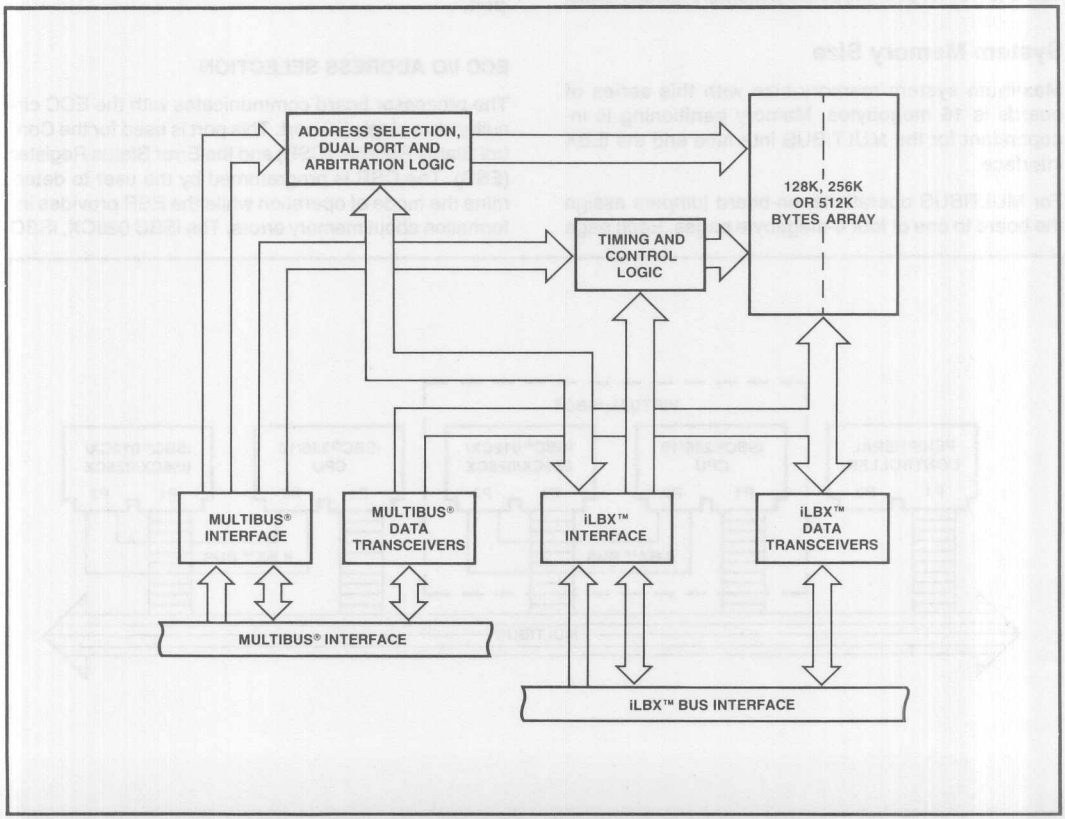


Figure 2. iSBC® 028CX/056CX/012CX Block Diagram

Diagnostic Mode — This mode is used for testing the on-board ECC circuitry. In this mode the write enable strobe to the ECC RAM array is continuously disabled. The diagnostic mode can be used to simulate errors and in conjunction with the "Examine Syndrome Word Mode" examine the check bits generated by the ECC circuitry.

Examine Syndrome Word Mode — This mode, in conjunction with the diagnostic mode, is used for testing the ECC memory. In this mode, the syndrome bits/check bits are clocked into the ESR on every memory read/write cycle, respectively. The ESR translation PROM switches to a transparent mode in the examine syndrome word mode. This allows the actual syndrome word generated by the 8206 ECC device to be examined.

ERROR STATUS REGISTER

This 8-bit register contains information about memory errors. The ESR reflects the latest error occurence. Table 1 shows the status register format. Bits 5 and 6 show the failing row while bits 0 through 4 indicate which bit (of the 16-bit data word or the 6-bit ECC syndrome word) is in error. Bit 7 is always high.

Bit 6	Bit 5	Meaning	
0	0	Error in row	0
0	1		1
1	0		2
1	1		3

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Meaning	
0	0	0	0	0	Error in data bit	0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0		8
0	1	0	0	1		9
0	1	0	1	0		10
0	1	0	1	1		11
0	1	1	0	0		12
0	1	1	0	1		13
0	1	1	1	0		14
0	1	1	1	1		15
1	0	0	0	0	Error in check bit	0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1		5
1	1	1	1	0	No Error	
1	1	1	1	1	Non-correctable (multiple-bit error)	

NOTE: Bit 7 is always high

Table 1. Error Status Register Format

Battery Back-up/Memory Protect

An auxillary power bus is provided to allow separate power to the RAM array for systems requiring backup of read/write memory. An active low TTL compatible memory protect signal is brought out on the auxillary bus connector which, when asserted, disables read/write access to the RAM board. This input is provided for the protection of RAM contents during system power-down sequences.

SPECIFICATIONS

Word Size Supported

8- or 16-bits

Memory Size

131,072 bytes (iSBC 028CX board)

262,144 bytes (iSBC 056CX board)

524,288 bytes (iSBC 012CX board)

Access Times (All densities)

MULTIBUS®

Read/Full Write — 380 ns (max)

Write Byte — 530 ns (max)

iLBX™ BUS

Read/Full Write — 300 ns (max)

Write Byte — 440 ns (max)

Cycle Times (All densities)

MULTIBUS®

Read/Full Write — 490 ns (max)

Write Byte — 885 ns (max)

iLBX™ BUS

Read/Full Write — 375 ns

Write Byte — 740 ns

NOTE: If an error is detected, read access time and cycle times are extended to 255 ns (max)

Refresh Cycle Time — 15.6 μs

Refresh Delay Time — 760 ns

Memory Partitioning

Maximum System memory size is 16M Bytes for both MULTIBUS and iLBX BUS. MULTIBUS partitioning is by Page, Block and Base, while the iLBX BUS is by Block and Base only.

PAGE ADDRESS

MULTIBUS® — 0-4 megabytes; 4-8 megabytes; 8-12 megabytes; 12-16 megabytes

iLBX™ BUS — N/A

BLOCK ADDRESS

Board	MULTIBUS® (16K Bytes)	iLBX™ Bus (64K Bytes)
iSBC® 028C	8 contiguous 16K byte blocks	2 blocks of 64K bytes
iSBC® 056C	16 contiguous byte blocks	4 blocks of 64 bytes
iSBC® 012C	32 contiguous 16K byte blocks	8 blocks of 64K bytes

NOTE: Blocks cannot cross 4M byte boundary

BASE ADDRESS

MULTIBUS® — Any 16K byte boundary

iLBX™ BUS — Any 64K byte boundary

Power Requirements

Voltage — 5VDC ± 5%

Board	Current	Standby (Battery Backup)
iSBC® 028CX	3.8A (typ.) 6.5A (max.)	2.0A (typ.) 2.2A (max.)
iSBC® 056CX	4.0A (typ.) 6.6A (max.)	2.1A (typ.) 2.3A (max.)
iSBC® 012CX	4.4A (typ.) 6.8A (max.)	2.3A (typ.) 2.5A (max.)

Environmental Requirements

Operating Temperature — 0°C to 55°C

Operating Humidity — To 90% without condensation

Physical Dimensions

Width — 30.48 cm (12 inches)

Height — 17.15 cm (6.75 inches)

Thickness — 1.27 cm (0.50 inches)

Weight — iSBC 028CX: 4699 gm (16.7 ounces); iSBC 056CX: 5329 gm (19.0 ounces); iSBC 012CX: 6589 gm (23.5 ounces)

Reference Manuals

145158-001 — iSBC 028CX/iSBC 056CX/iSBC 012CX Hardware Reference Manual

144456-001 — Intel iLBX Specification

9800683-03 — Intel MULTIBUS Specification

Manuals may be ordered from any Intel Sales Representative, Distributor Office or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

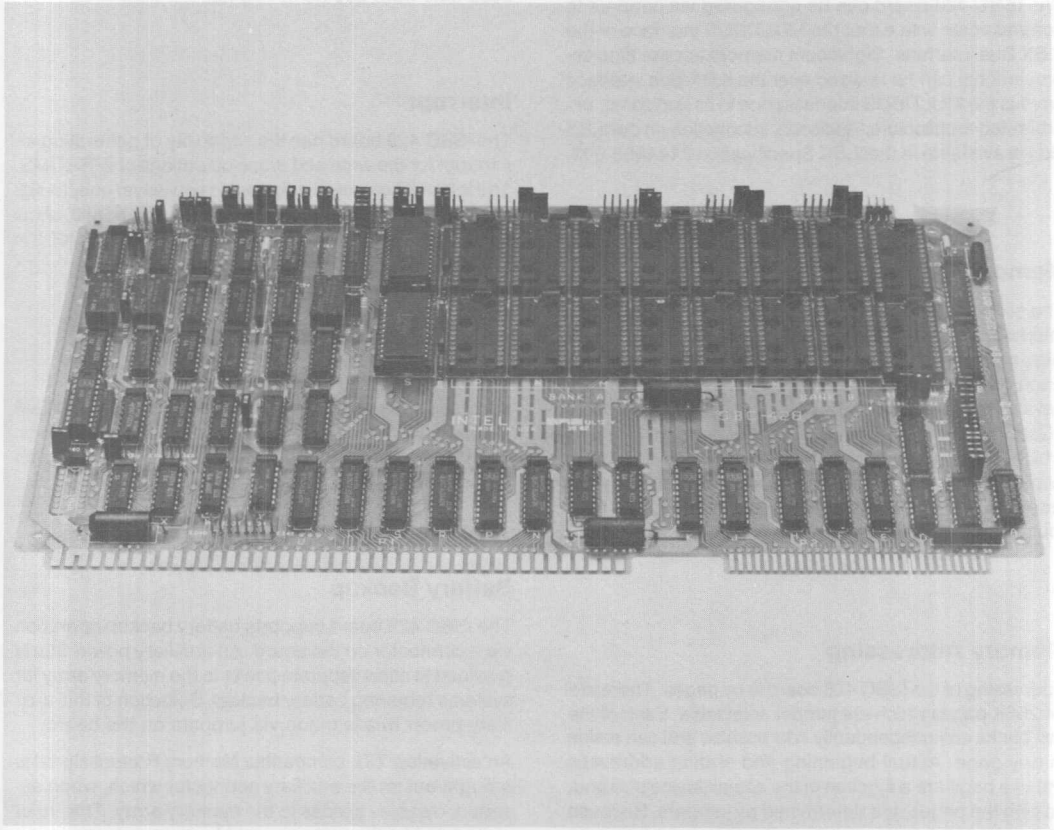
ORDERING INFORMATION

Part Number	Description
iSBC 012CX	512K byte RAM board with iLBX
iSBC 056CX	256K byte RAM board with iLBX
iSBC 028CX	128K byte RAM board with iLBX

iSBC® 428 UNIVERSAL SITE MEMORY EXPANSION BOARD

- **Supports EPROM, ROM, E²PROM, SRAM, IRAM and NVRAM**
- **iLBX™ BUS or MULTIBUS® Selectable**
- **Provides support for Battery Backup/ Memory Protect**
- **Sixteen 28 pin Universal sites**
- **Assignable anywhere within a 16 megabyte address space on 256K byte boundaries**
- **Jumper selectable base address on 4K byte boundaries**

The iSBC® 428 Universal Site Board is a member of Intel's complete line of Memory and I/O Expansion boards. The iSBC 428 Universal Site Memory Expansion Board interfaces directly to the iSBC 80, iSBC 88, or iSBC 86 Single Board Computers via the MULTIBUS® System Bus to expand system memory requirements, while system memory expansion requirements for iSBC 286 Single Board Computer can interface via either the MULTIBUS or the high speed iLBX™ Bus.



FUNCTIONAL DESCRIPTION

General

The iSBC 428 board contains sixteen 28 pin sockets. The actual capacity of the board is determined by the type and quantity of components installed by the user. The iSBC 428 board is compatible with five different types and densities of devices: the 2K by 8 thru 64K by 8 EPROM/ROM devices, 2K by 8 thru 8K by 8 "Five Volt Only, Enhanced" E^2PROM devices, 512 by 8 thru 16K by 8 NVRAM (Non-Volatile RAM) devices, 2K by 8 thru 32K by 8 SRAM devices, and 8K by 8 IRAM (Integrated RAM) devices. In addition the board can be accessed by either the MULTIBUS System Bus or Intel's new high speed iLBX Bus.

iLBX™ Bus

The iSBC 428 board can be configured via jumpers to communicate with either the MULTIBUS interface or the iLBX Bus interface. Significant memory access time improvements can be realized over the iLBX Bus interface (versus the MULTIBUS interface) due to its dedicated, unarbitrated architecture. Additional information on the iLBX Bus is available in the iLBX Specification #144456-003.

Memory Banks

The sixteen sites on the iSBC 428 board are partitioned into two banks of 8 sites each. Within each bank the 8 sites are further partitioned into 2 groups of 4 sites each. Each group of 4 sites is configurable to each of the six device types described above via a "Configurator". The "Configurator" is an arrangement of push-on jumpers which configures each of the four groups of 4 sites. Within each bank devices of the same density must reside and within each group devices of the same type must reside (i.e. SRAM or EPROM).

Memory Addressing

Addressing of the iSBC 428 board is by pages. There are 64-256K pages which are jumper selectable. Each of the two banks are independently addressable and can reside in any page. Actual beginning and ending addresses within a page are a function of the actual device size and, as with the pages, are determined by jumpers. Because of the paging based memory addressing architecture more than one iSBC 428 board can be placed in a system.

Mode of Operation

The iSBC 428 board can operate in one of two modes: the 8 bit only mode or the 8/16 bit mode. The 8 bit mode provides the most efficient memory configuration for systems handling 8 bit data only. The 8/16 bit mode allows the iSBC 428 board to be compatible with systems employing 8 bit and 16 bit masters. The mode of operation is selected by on board jumpers and is available for both MULTIBUS and iLBX Bus configurations.

Memory Access

The iSBC 428 board has jumper selectable access times which allows the board to be tailored to the performance of the particular devices which are installed in the iSBC 428 board. The board can be configured via jumpers to accept devices with an access time range of 50 ns to 500 ns with a granularity of 50 ns and results in a board access time from 225 ns to 775 ns.

Interrupt

The iSBC 428 board has the capability of generating an interrupt for the write and erase operations of E^2PROMS. The interrupt can be configured in two ways: one, to signal completion of the E^2PROM write cycle, or two, allow polling by the system to determine the status of the E^2PROM during the write programming time.

Inhibits

Inhibits are provided on the iSBC 428 board to allow ROM to overlay RAM for bootstrapping or diagnostic operations. Each bank of the iSBC 428 board can be overlayed with the system RAM by jumpers provided on the board.

Battery Backup

The iSBC 428 board supports battery backup operation via a connector on the board. An auxiliary power bus is provided to allow separate power to the memory array for systems requiring battery backup. Selection of this auxiliary power bus is made via jumpers on the board.

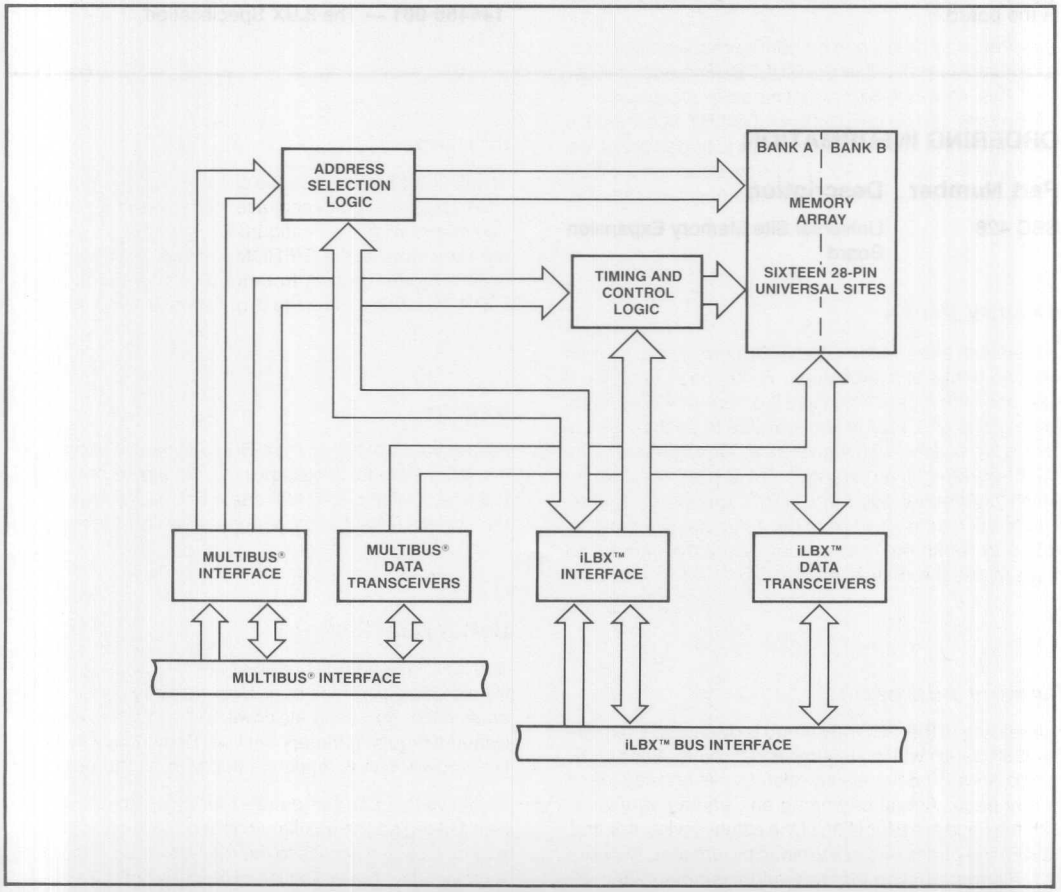
An active-low TTL compatible Memory Protect signal is brought out on the auxiliary connector which, when asserted, disables access to the memory array. This input is provided for the protection of Memory contents during system power-down sequences.

Devices Supported

Listed below are the current and future devices supported by the iSBC 428 board.

	Size							
Type	**512 x 8**	**2K x 8**	**4K x 8**	**8K x 8**	**16K x 8**	**32K x 8**	**64K x 8**	**Comments**
EPROM	—	2716	2732A	2764	27128	27256	X	—
ROM	—	X	X	X	X	X	X	—
EEPROM	—	2817A	X	X	X	X	—	5V, Enhanced
SRAM	—	X	X	X	X	X	—	NMOS & CMOS
NVRAM	—	X	X	X	—	—	—	—
IRAM	—	—	—	2186	—	X	—	—

X-Denotes that the iSBC 428 board will support the device indicated but that it is not currently available from Intel.



iSBC® 428 Block Diagram

SPECIFICATIONS

Word Size

8 or 8/16 bits

Memory Size

Sockets are provided for up-to sixteen 28 pin devices which can provide up to 512K bytes of EPROM/ROM/SRAM.

Access Time

Jumperable from 225 to 775 ns with a granularity of 50 ns and is equivalent for both MULTIBUS and the iLBX Bus.

Power Requirements

$V_{CC} = 5$ volts $\pm 5\%$

$I_{CC} = 2.0$ amps, maximum, without any memory devices in the board.

Physical Characteristics

Length — 30.48 cm (12 inches)

Width — 17.15 cm (7.05 inches)

Depth — 1.27 cm (0.5 inches)

Environment

Operating Temperature — 0°C to +55°C

Relative Humidity — 90% non-condensing

Reference Manual

145696-001 — iSBC 428 Hardware Reference Manual (NOT SUPPLIED)

Additional Literature

9800683-04 — MULTIBUS Specification

144456-001 — The iLBX Specification

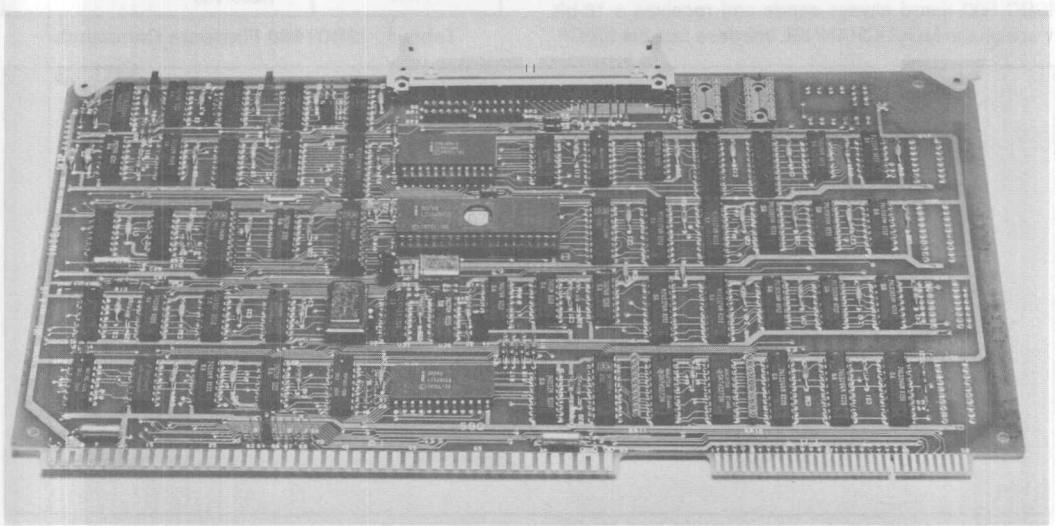
ORDERING INFORMATION

Part Number	Description
SBC 428	Universal Site Memory Expansion Board

iSBC® 580 MULTICHANNEL™ BUS TO iLBX™ BUS INTERFACE

- **MULTICHANNEL™ I/O bus 16-bit Talker/Listener interface**
- **iLBX™ bus master interface (primary or secondary)**
- **Supports MULTIBUS® interrupts**
- **Data rates up to 5.3 megabytes per second**
- **Addresses up to 16 megabytes of iLBX™ bus memory**
- **MULTIBUS® form factor**

The iSBC® 580 Interface Board is a member of Intel's complete line of MULTIBUS® microcomputers which maximize system performance by using separate optimized buses for intra-system communication (MULTIBUS system bus), high speed I/O (MULTICHANNEL™ DMA I/O bus), expansion I/O (iSBX™ I/O expansion bus) and high-speed memory expansion (iLBX™ execution bus). The iSBC 580 board provides a key element in the enhanced MULTIBUS system architecture by implementing a MULTICHANNEL I/O bus to iLBX bus interface on a single 6.75 × 12.00 inch printed circuit board. Using an LSI state machine with standard on-chip firmware to maximize throughput, the on-board Intel® 8048 Single Component Microcomputer transfers data between a MULTICHANNEL Controller, device and up to 16 megabytes of iLBX bus resident memory at rates up to 5.3 megabytes per second. Acting as a MULTICHANNEL Talker/Listener, the iSBC 580 board increases the system's overall performance by transferring data between the MULTICHANNEL I/O bus and system memory without using the MULTIBUS system bus. As shown in Figure 1, this allows other system tasks to utilize MULTIBUS resources while high-speed I/O block transfers are occurring simultaneously. The board's high throughput and independence from MULTIBUS activities make it an ideal solution for applications that must transfer large amounts of data in and out of a MULTIBUS system, such as MULTIBUS to host computer links and mass storage, graphics display and high-speed data acquisition subsystem interfaces.



FUNCTIONAL DESCRIPTION

MULTICHANNEL™ Interface Capabilities

The MULTICHANNEL I/O bus is designed to provide a general purpose, high-speed data path between a microcomputer system and up to 15 block transfer devices. Using a 16-bit wide data bus and a simple asynchronous handshaking scheme, the MULTICHANNEL bus can operate over distances up to 15 meters (50 feet) with a maximum burst throughput of 8 megabytes/second. The bus consists of 16 address/data lines, 6 control lines, 2 interrupt lines, parity lines and reset. Via these signals, a MULTICHANNEL Supervisor or Controller may configure and then initiate a block data transfer with any other device on the bus.

The iSBC 580 board acts as a 16-bit only Talker/Listener device on the MULTICHANNEL I/O bus. As a Talker/Listener, the board will respond to Register Read or Write and DMA requests issued by the MULTICHANNEL Supervisor (typically an iSBC 589 board) or by a MULTICHANNEL Controller device.

The iSBC 580 board implements 32 MULTICHANNEL Device Registers. The first three registers are the standard STO Status, SRQ Status and SRQ Mask Registers, as defined by the MULTICHANNEL Bus Specification. The remaining registers are used to communicate with the on-board firmware and for user data storage. The firmware operations which may be initiated by writing to the Command Register are listed in Table 1. The iSBC 580 board always sends and receives a 16-bit word on the MULTICHANNEL interface but, the iSBC® 580 device registers (see Table 2) are 8-bit only. Register Write operations use only the low order 8-bits (AD0-AD7). Register Read operations place the data on the low order data lines of the MULTICHANNEL I/O bus and set the high order data lines to FFH.

Command Code (Hex)	Operation
0	No Operation
1	Go off line forever
2	STO poll (diagnostic)
3	SRQ poll (diagnostic)
4	Set on-board timer
5	Read on-board timer
6	Start on-board timer
7	Stop on-board timer
8	Generate Task Complete interrupt
9	Perform checksum on firmware (diagnostic)
A	Turn on-board LED on
B	Turn on-board LED off
C	Reset
D, E	Reserved
F	Set interrupt mask
10	Read interrupt mask
11-1F	Reserved

Table 1. iSBC® 580 Firmware Commands

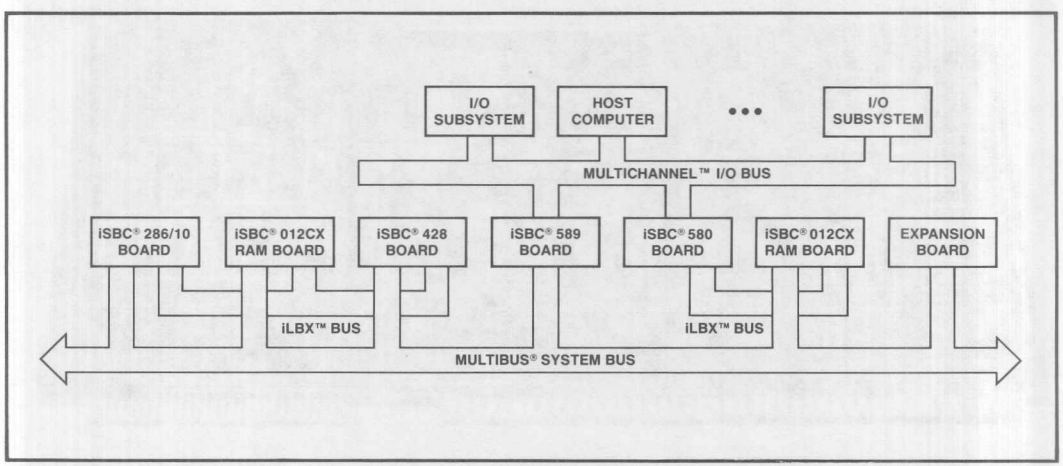


Figure 1. iSBC® 580 board, configured as an iLBX™ Bus Primary Master, transfers data between iLBX™ memory and MULTICHANNEL™ devices without using the system bus. The iSBC® 589 board acts as the MULTICHANNEL™ Supervisor and performs data transfers between MULTIBUS® memory and MULTICHANNEL™ devices.

The iSBC 580 board can generate maskable MULTICHANNEL STO interrupts when the board detects a parity error in incoming MULTICHANNEL data, when the board attempts to address non-existent iLBX memory or when the board detects a MULTIBUS interrupt from the system in which it resides. The last type of interrupt allows a single board computer to send an interrupt via the iSBC 580 board to the MULTICHANNEL Supervisor located in another MULTIBUS system. The board can also generate a number of SRQ interrupts on the MULTICHANNEL bus as shown in Figure 2.

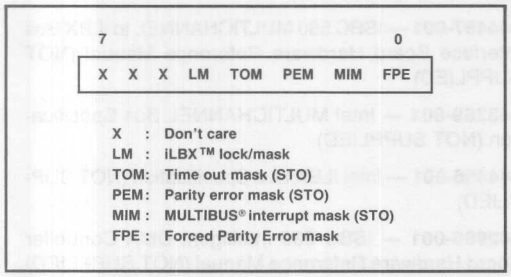


Figure 2. iSBC® 580 Interrupt Mask Register (14H)

iLBX™ Bus Interface Capabilities

Used in conjunction with the MULTIBUS interface, the iLBX bus is designed to provide off-board memory and I/O expansion for single board computers while maintaining on-board performance. The iLBX bus provides high-speed access to compatible expansion boards by granting privileged use of the bus to a single Primary Master. The bus also provides limited access to iLBX bus expansion boards for, at most, one Secondary Master that requires only occasional or non-concurrent access to iLBX resources. The iLBX bus, with 16 data lines, 24 address lines plus control, parity and interrupt signals, utilizes all the pins on the P2 connector except the four pins dedicated to the high-order address lines of the MULTIBUS interface. The non-multiplexed address and data lines provide access to up to 16 megabytes of iLBX bus resident memory, on up to 4 separate expansion boards, at speeds comparable to that of a single board computer's on-board resources.

The iSBC 580 board is configurable as either a Primary or a Secondary Master on the iLBX bus. Figure 1 shows a typical system configuration, with an iSBC 580 board acting as a Primary Master. The board can access up to 16 megabytes of iLBX memory. Supporting 16-bit transfers on the MULTICHANNEL bus, the board accesses memory as 16-bit words on even byte iLBX address boundaries. To increase the performance of iLBX memory read operations, the iSBC 580 board prefetches data from memory while the current data word is being transferred over the MULTICHANNEL I/O bus.

Register	Address
STO Status	00H
SRQ Status	01H
SRQ Mask	02H
RESERVED	03H-0FH
General Purpose Registers	10H*-1FH

* **NOTE:** 10H used as Command Register.

Table 2. iSBC® 580 MULTICHANNEL™ Device Register Set

SPECIFICATIONS

MULTICHANNEL™ Bus

Interface — Basic Talker/Listener

Transfer Mode — 16-bit

Device Address — Jumper selectable between 00H and 0EH

Registers — STO status, SRQ status, SRQ mask plus device specific registers

Signal Level — TTL compatible

iLBX™ Bus

Interface — Primary or Secondary (default) Master

Transfer Mode — 16-bit

Addressing — 16 megabytes on even byte boundaries only

Signal Level — TTL compatible

MULTIBUS® Interface

Data — None

Addressing — None

Interrupts — Jumper configurable to use any 1 of the 8 MULTIBUS interrupt lines. Interrupts are edge triggered.

Signal Level — TTL compatible

Throughput

5.3 megabytes/sec (2.65 megatransfers) max.

Connectors

iLBX™ BUS INTERFACE

Double-Sided Pins — 60

Centers — 0.100 in.

Mating Connectors* — Kelam RF30-2803-5
T&B Ansley A3020
(609-6025 modified)

MULTICHANNEL™ BUS INTERFACE

Pins — 60

Centers — 0.100 in.

Mating Connectors* — 3M 3334-6000
Berg 65949-960

* Connectors compatible with those listed may also be used.

Physical Characteristics

Width — 12.00 inches (30.5 cm)

Height — 6.75 inches (17.1 cm)

Depth — 0.60 inches (1.5 cm)

Weight — 12 ounces (340 gm)

Environmental Characteristics

Operating Temperature — 0° to 55°C

Relative Humidity — to 90% (without condensation)

DC Power Requirements

Voltage — +5 volt only ±5%

Current — 2.5 amps (typical)

Reference Manuals

144457-001 — iSBC 580 MULTICHANNEL to iLBX Bus Interface Board Hardware Reference Manual (NOT SUPPLIED)

143269-001 — Intel MULTICHANNEL Bus Specification (NOT SUPPLIED)

144456-001 — Intel iLBX Bus Specification (NOT SUPPLIED)

142996-001 — iSBC 589 Intelligent DMA Controller Board Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051

ORDERING INFORMATION

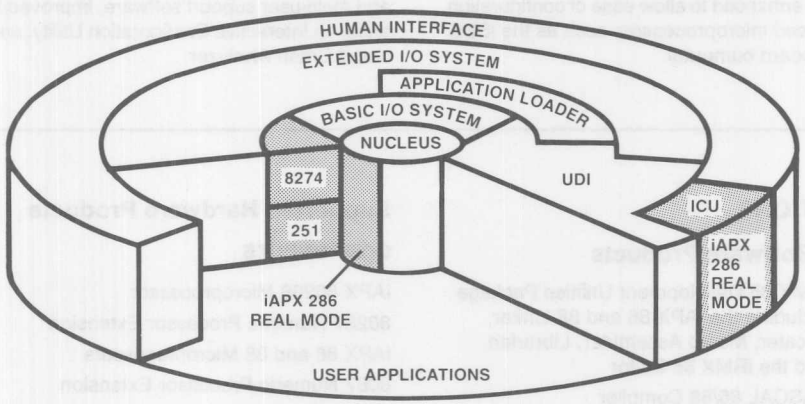
Part Number	Description
SBC 580	MULTICHANNEL to iLBX Bus Interface Board

iRMX™ 286R OPERATING SYSTEM

- **Real-Time Processor management for time critical iAPX 286 applications in Real Address Mode**
- **Higher performance, complete iRMX™ 86 compatibility**
- **Complete support of 80287 Processor Extension**
- **New terminal driver for 8274 Multi Protocol Serial Controller (MPSC)**
- **New iSBC® 251 Bubble Memory Driver**
- **Multi-terminal support with multi-user human interface**
- **On-target system development with Universal Development Interface (UDI)**
- **Configurable system size and function for diverse application requirements**
- **All iRMX™ 286R code can be (P)ROM'ed to support totally solid state designs**
- **Powerful utilities for interactive configuration and real-time debugging**
- **Functions in conjunction with iRMX™ 86 Release 5**

The high performance iRMX™ 286R Operating System, functioning in conjunction with the iRMX 86 Release 5 Operating System software, is designed to manage and extend the resources of iSBC® 286 Single Board Computers as well as other iAPX 286-based Microcomputers in Real Address Mode. The iRMX 286R Operating System is an easy-to-use, real-time, multi-tasking and multi-programming software system providing the capability of executing the entire configurable layers of the iRMX 86 software in the Real Address Mode of the iAPX 286 and the iSBC 286/10 Single Board Computer.

The new features added to this incremental System include drivers for both channels of an 8274 and a driver for the iSBX™ 251 MULTIMODULE™ board.



NEW IN iRMX™ 286R

April, 1983

The iRMX™ 286R Operating System is a complete set of system software modules that provide resource management functions needed by most computer systems. These management functions are currently available to OEMs in Release 5 of the iRMX 86 Operating System. For a complete description of the functions, their value and performance, please refer to the Release 5 iRMX 86 Data Sheet (order number 210885-001).

This data sheet describes the new features provided by the iRMX 286R Operating System. These new features add new capabilities specially designed for OEMs wishing to take better advantage of the speed and performance of the recent VLSI microprocessor, the iAPX 286.

New drivers provided with the iRMX 286R Operating System include:

— An 8274 terminal device driver, to support the 8274 for two channel Async support of the iSBC® 286/10 board in RS232 mode.

— Support for the iSBX™ 251 Bubble Memory System, installed as a custom driver.

The 8274 terminal device driver supports two serial channels used in RS232 mode and supports all features of the iRMX 86 terminal support. To use the RMX debugger an iSBX 351 MULTIMODULE™ is required.

The iRMX 286R Operating System is a natural extension, growth path for iRMX 86 users offering a higher-performance, simple upgrade. The Interactive Configuration Utility has been enhanced to allow ease of configuration of iAPX 286 based microprocessors such as the iSBC 286/10 single board computer.

FUNCTIONAL DESCRIPTION

To take best advantage of the iAPX 286 microprocessor in applications where computers are required to perform many functions simultaneously, the iRMX 286R Operating System provides a multi-programming environment in which many independent, multi-tasking application programs may run. Each application environment may be treated separately to allow application programmers the flexibility to separately manage each application's resources while developing and testing the software for each independently.

The resource management functions of the iRMX 286R System are supported by a number of configurable software layers. While many of the functions supplied by the innermost layer, the Nucleus, are required by all systems, all other functions are optional. The I/O systems, for example, need not be included in systems with no secondary storage requirement. Each layer provides functions that encourage application programmers to maintain an understandable structure and to develop easily maintainable programs more quickly.

The components of the iRMX 286R Operating System provide both implicit and explicit management of a system's resources. These resources often include the processor's time and registers, the 80287 Numeric Data Processor Extension, up to one megabyte of system memory, up to 57 independent interrupt sources, all input and output devices, as well as directory and data files contained on mass storage devices. The Operating System makes it easier for designers to include many terminals in their systems by providing multi-terminal and multi-user support software, improved I/O performance, an Interactive Configuration Utility, and a sophisticated Crash Analyzer.

SPECIFICATIONS

Supported Software Products

iRMX 860	iRMX 86 Development Utilities Package including the iAPX 86 and 88 Linker, Locater, Macro Assembler, Librarian, and the iRMX 86 Editor
iRMX 861	PASCAL 86/88 Compiler
iRMX 862	FORTRAN 86/88 Compiler
iRMX 863	PL/M 86/88 Compiler
iRMX 864	TX-Screen-Oriented Editor
iMMX 800	MULTIBUS® Message Exchange software package for iRMX 80, 86, and 88 application systems

Supported Hardware Products

COMPONENTS

iAPX 80286 Microprocessor
80287 Numeric Processor Extension
iAPX 86 and 88 Microprocessors
8087 Numeric Processor Extension
80130 Operating System Firmware Component
8253 and 8254 Programmable Interval Timers
8259A Programmable Interrupt Controller
8251A USART
8255 Programmable Parallel Interface
8274 USART 2 Channel (Serial) Controller

Order Number: 210898-001

iSBC® MULTIBUS® PRODUCTS

iSBC 86/12A, 86/05, 86/14, 86/30, 88/25, 88/40, and 286/10 Single Board Computers

iSBC 204 Flexible Disk Controller

iSBC 206 Hard Disk Controller

iSBC 208 Flexible Disk Controller

iSBC 215 Winchester Disk Controller

iSBC 220 SMD Disk Controller

iSBC 251 Bubble Memory System

iSBC 254 Bubble Memory System

iSBC 534 4-Channel Terminal Interface

iSBC 544 Intelligent 4-Channel Terminal Interface and Controller

iSBX 218 Flexible Disk Controller

iSBX 350 Parallel Port (Centronix-type Printer Interface)

iSBX 351 Serial Communications Port

iSBX 270 CRT, Light Pen and Keyboard Interface

Available Literature

iRMX 286R Operating System Installation and Configuration Guide for Release 1 (145556-001)

All of the manuals listed below are supplied with iRMX 86 Release 5 and are available separately under the order numbers shown.

Introduction to the iRMX 86 Operating System (9803124-04)

iRMX 86 Operator's Manual (144523-001)

Master Index for iRMX 86 Release 5 Documentation (145015-001) (Not available until 1983)

Getting Started With The Release 5 iRMX 86 System (145073-001)

iRMX 86 Installation Guide (9803125-05)

iRMX Configuration Guide (9803126-05)

iRMX 86 Nucleus Reference Manual (9803122-04)

iRMX 86 Terminal Handler Reference Manual (143324-002)

iRMX 86 Debugger Reference Manual (143323-002)

iRMX 86 Basic I/O System Reference Manual (9803123-05)

iRMX 86 Loader Reference Manual (143318-002)

iRMX 86 Extended I/O System Reference Manual (143308-002)

iRMX 86 Human Interface Reference Manual (9803202-003)

Guide to Writing Device Drivers for the iRMX 86 and iRMX 88 I/O Systems (142926-004)

iRMX 86 Programming Techniques (142982-003)

User's Guide for the iSBC 957B, iAPX 86, 88 Interface and Execution Package (143979-002)

iRMX 86 Disk Verification Utility Reference Manual (144133-002)

Runtime Support Manual for iAPX 86, 88 Applications (121776-002)

iRMX 86 Crash Analyzer Reference Manual (144522-001)

ORDERING INFORMATION

The iRMX 286R facilities described in this data sheet require the iRMX 86 R5 Operating System as a prerequisite.

For all new iRMX users, there are a number of different licensing and support options available. All options are provided on either single or double density ISIS-formatted diskettes, on 5¼" iRMX 86-formatted diskettes, or on double density iRMX 86-formatted diskettes. ISIS-format diskettes may be used on Intel Intellec® Development Systems. The iRMX 86-format may be used on any iRMX 86-based system supporting the appropriate compilers and development environment.

The OEM license options listed here allow users to incorporate the iRMX 286R Operating System into their applications. Each use requires payment of an Incorporation Fee.

Other licensing options include prepayment of future incorporation fees, single use rights for a single machine, support at a second development site, and one-year support service extensions.

Each option includes 90 days of update service that provides Software Problem Report Service and copies of System updates that occur during this period. All initial licenses include the iSDM™ 286 System Debug Monitor and iRMX 286R documentation.

As with all Intel Software, purchase of any of these options requires execution of a standard Intel Master Software License.

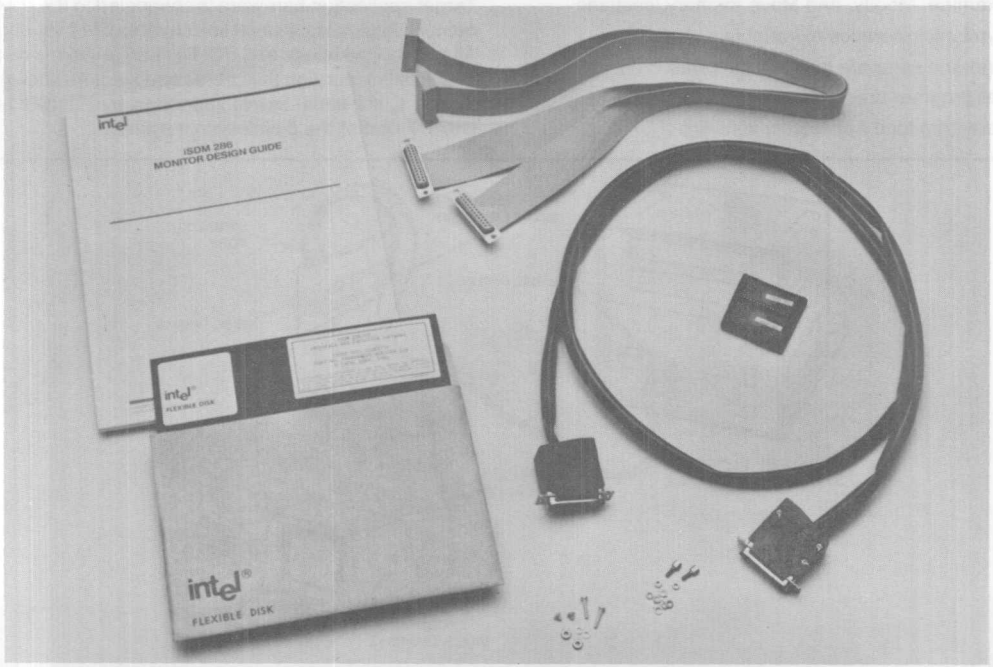
Part Number	Description
RMX 286R KIT ARO	Single Density, OEM License
RMX 286R KIT BRO	Double Density, OEM License
RMX 286R KIT ERO	Double Density, iRMX 86-format, OEM License for use on iRMX 86-based environments

NOTE: Each option requires previous purchase of iRMX 86 Release 5. iRMX 286R does not support the Protected Virtual Address Mode (PVAM) of the iAPX 286-based microprocessor.

iSDM™ 286
iAPX 286 SYSTEM DEBUG MONITOR

- **Development support of iSBC® 286-and iAPX 286-based applications**
- **Real Address Mode (RAM) and Protected Virtual Address Mode (PVAM) support**
- **Universal Development Interface (UDI) support via development system connection**
- **Underlying debugging tool for iRMX™ 286R applications**
- **Supports 80287 Numeric Processor Extension (NPX) for high-speed math applications**
- **Program load capability from Intellec® Series III Development Systems**
- **Bootstrap Loader for iRMX™ 286R, 86, and 88 file compatible peripherals**
- **iAPX 286 single step operation allowed**

The Intel iSDM™ 286 System Debug Monitor package contains the necessary hardware, software, cables, PROMs, and documentation required to interface an iSBC® 286 board or iAPX 286 component applications to an Intellec® Series III through a high-speed link. The System Debug Monitor supports an OEM's choice of the iRMX™ 286R Real-Time Multitasking Operating System or custom operating system, with debugging tools to examine CPU registers, memory content, CPU descriptor tables, and other crucial environmental details. The Monitor also allows programs to access files on the development system via the internal UDI support and the serial communication link.



FUNCTIONAL DESCRIPTION

Overview

The iSDM 286 System Debug Monitor provides programmers of iAPX 286-based applications with the debugging tools needed to test new applications ranging from single-user systems to complex operating systems. Programmers are given direct access to both the Real Address (ram) and Protected Virtual Address (pvam) Modes of the CPU via a simple terminal interface, or via an Intellec Series III Development System.

Universal Development Interface

Any iRMX 86, Series III, or other UDI-based application can be supported by the iSDM 286 Monitor. The Monitor emulates many of the UDI calls (ram or pvam), and passes all requests for a file system to the host development station. UDI applications such as compilers and other programs available from Independent Software Vendors can be tested in the target iAPX 286 environment immediately.

Powerful Debugging Commands

A powerful set of user functions includes commands to:

- Examine and Modify CPU Registers
- Examine, Modify, and Move memory locations
- Symbolic reference to variable names
- Find and compare memory contents
- Set program breakpoints
- Bootstrap load application software
- Single-step CPU operation
- Change between Real Address Mode and Protected Virtual Address Mode

Formatted Displays

The iSDM 286 Monitor formats all iAPX 286 pre-defined data structures into clearly understandable displays. This display gives programmers a formatted view of CPU registers such as LDTs, GDTs, IDTs, Segment Selectors, and Task State Segments — not just a series of unconnected digits.

Numeric Data Processor Support

In addition to executing 80287 Numeric Processor Extension (NPX) applications with full NPX performance, programmers may examine and modify NPX registers using decimal and real number format. Any location in memory known to contain numeric values in standard real format (IEEE P754) may be examined or modified using normal decimal notation. In this manner programmers may feel confident that correct and meaningful numbers are available to applications without having to encode and decode complex real, integer, and BCD hexadecimal formats.

High-Speed Serial Connection

Target application hardware is connected to the development system via a serial link capable of 19.2K baud. All control operations and UDI file manipulations occur over this link through the cables supplied. As shown in Figure 1, the serial link is supported by the iSBC 86 USART port of the development system.

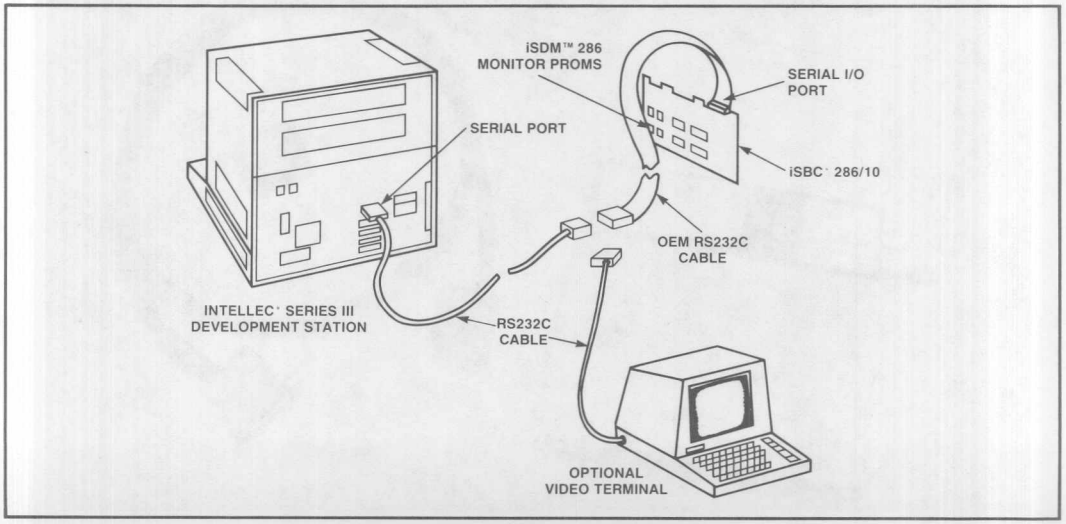


Figure 1. Typical iSDM™ 286 Environment

SPECIFICATIONS

Development System Environment

Intellec MDS Series III with 64 KBytes.

Target System Environment

Any iAPX 286 system with 8274 (non-vectored mode) serial link, 8254 timer, and 8259A interrupt controller such as the iSBC 286/10 Single Board Computer.

PROMs are supplied for locations 0FF8000H through 0FFFFFFH.

ORDERING INFORMATION

Part Number	Description
SDM 286	iSBC 286 and iAPX 286 System Debug Monitor package including cables, PROMs, software, and operator manual (Not available stand alone until Q3'83) A software license must be or have been executed Currently available only with the iSBC 286/10 ES Kit or with the iRMX 286R Kit.